A Linear Tunable Amplifier for Implantable Neural Recording Applications

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***Abstract*— A fully integrated tunable low-noise amplifier for neural recording applications is presented that is highly linear over the entire signal band. A modified system design is presented to optimize the area/noise/linearity performance. A novel pseudo-resistor with improved linearity is also proposed. This design, simulated in a 0.18-µm CMOS process, consumes 41.4 µW from a 1.8-V supply. The simulated integrated input-referred noise is 2.61 μV_{rms} over 300 Hz to 10 kHz. The amplifier also provides an output swing of 1 V_{P-P} with a total harmonic distortion of -43.61 dB at 300 Hz and -46.41 dB at 10 kHz.**

I. INTRODUCTION

Bio-potential amplifier is one of the most critical blocks in neural recording systems used by neuroscientists in various biomedical applications including brain–machine interface and neural prostheses. The main challenges in the design of the analog front-end of sensor interface (SI) circuits are derived from the nature of neural signals. Due to the small amplitude of neural signals, amplification must be performed before these signals can be digitized or analyzed. An integrated front-end amplifier (FEA) for neural signals must have sufficiently low input-referred noise to detect signals as small as a few tens of micro-volts in amplitude. Also the amplifier must have sufficient dynamic range for large-amplitude input signals (1-2 mV). The input impedance of the SI must be higher than the equivalent impedance of the electrode-tissue interface. The frequencies of neural signals span from a few hertz to a few kilo hertz. Therefore, the amplifier must amplify the signals in the band of interest while introducing a large enough dynamic range. Furthermore, the electrode-tissue interface usually inserts a high DC offset in the input signal which has to be removed by a high-pass filter not to saturate the amplifier [1]-[3]. Also, the amplifier should have a high common-mode and power-supply rejection ratios to minimize any interference from 50/60 Hz power line noise and power supply noise. If tissue cells are exposed to elevated temperatures for a long time, they will be destroyed. Thus, the SI circuit must operate at low power levels to minimize tissue heating. In addition, the SI circuit should consume little silicon area and use few off-chip components to minimize the size [3].

Since the peak amplitude of the neural signals varies based on the electrode type and conditions, the gain of the amplifier must be programmable. Also, the amplifier circuit parameters, e.g. the values of the resistors and the parameters of the operational transconductance amplifier (OTA) may change with process variations. Therefore, the bandwidth of the amplifier must be tunable as well. Note that the temperature of the implantable SI circuit is almost constant [3].

Another design issue in SI circuit is the linearity of the amplifier. Not only the linearity of the resistors, usually implemented employing MOS pseudo-resistors, but also the tracking error of the amplifier affect the linearity of the FEA. Although several attempts have been reported to decrease the power consumption and increase the signal-to-noise-ratio (SNR) of biomedical sensor interface systems [1]-[4], only a few works have discussed the linearity of these systems [2, 5].

This paper presents an integrated tunable neural recording sensor interface amplifier. The structure of the FEA including a low-noise amplifier, a tunable band-pass filter and a variable gain amplifier (VGA) is modified in order to optimize the noise, linearity and area performance. Also a novel pseudo cross-coupled tunable pseudo-resistor structure is introduced for the adjustment of low-cutoff frequency of the amplifier.

The paper is organized as follows: section II describes the challenges in the system architecture and design, proposed pseudo cross-coupled resistor and its comparison with the previous works. Section III reports the simulation results, and section IV concludes the paper.

II. SENSOR INTERFACE CIRCUIT DESIGN

In this section, design considerations of a low-noise front-end amplifier for neural recording system with low- and high-cutoff frequencies of 300 Hz and 10 kHz will be discussed. The overall system gain should be programmable with a nominal value of 54 dB. Using a 0.18 µm CMOS technology with a supply voltage of 1.8 V, the output swing is chosen to be 1 V_{p-p}. Since the output of the amplifier is digitized using a successive approximation register (SAR) analog-to-digital converter (ADC), the amplifier should be able to drive a switched capacitor of 20 pF.

In literature several reports have been presented to implement FEAs for implantable biomedical devices both in single-stage [3, 4, 5, 7, 8] and multi-stage architecture [1, 2, 6]. The capacitively-coupled amplifier that is employed in the stages of the amplifier shown in Fig.1 is commonly used to achieve good trade-offs between the performance, power, and area and to make the design of tunable and reconfigurable band-pass filters easier [2]. The choice of the number of the stages of the amplifier and the specifications of each stage greatly affects the overall system performance. The system design methodology proposed in this paper will be discussed in sub-section A. Furthermore, since the resistance of the employed resistors in such low-frequency applications is extremely high, realizing the resistors is another design challenge. MOS pseudo-resistors that occupy very small area are good candidates for the real resistors [7]. The main

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