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# A LOW POWER FULLY INTEGRATED BANDPASS OPERATIONAL AMPLIFIER FOR BIOMEDICAL NEURAL RECORDING APPLICATIONS

Pedram Mohseni and Khalil Najafi
Center for Wireless Integrated MicroSystems (WIMS)
Department of Electrical Engineering and Computer Science
University of Michigan, Ann Arbor, MI 48109-2122 USA

Abstract- **This paper presents a low power fully integrated bandpass amplifier for a variety of biomedical neural recording applications. A standard two-stage CMOS amplifier in a closed-loop resistive feedback configuration provides stable AC gain of 39.5 dB at 1 kHz. A PMOS input transistor, biased near the sub-threshold region acting as a high value resistor in the range of hundreds of mega ohms, is utilized to clamp the large and random DC open circuit potential that normally exists at the electrode-electrolyte interface. The 3 dB bandwidth of the amplifier is measured to be 26 Hz – 6.5 kHz and the tolerable DC input range is measured to be at least 1 V. The amplifier measures 0.107 mm$^2$ in die area and dissipates 133 μW from a 3 V power supply. It is fabricated in MOSIS AMI 1.5 μm double poly double metal n-well CMOS process. Bench tests show complete functionality of the amplifier in both light and dark conditions and for a wide range of recording electrode capacitance.**

Keywords- **Low power, fully integrated, bandpass amplifier, sub-threshold operation, neural recording.**

## I. INTRODUCTION

In biomedical neural recording applications some level of amplification is always necessary before any further signal processing can be performed due to the low level amplitude of recorded neural signals. However, there are several challenges involved in the design of low power, fully integrated, and stable operational amplifiers as the front-end of neural recording circuitry. Ji *et al.* have designed and tested one type of these amplifiers in an implantable CMOS interface with microelectrode arrays [1]. Their amplifier provides a mid-band gain of about 51 dB without amplifying the DC components. However, one major issue with this design is the gain variability from probe to probe or even from channel to channel on the same probe. Gains also drift during probe use and by ambient light, which would eventually saturate the amplifier. All these problems arise from the fact that the amplifier does not incorporate standard AC feedback. The gain is actually the open-loop AC gain of the amplifier, which strongly depends on the current through several of the transistors and process parameters such as gate oxide thickness and transistor threshold voltage. Another major challenge in the design of the operational amplifier is the random DC open-circuit potential developed at the electrode-electrolyte interface. It can be as high as ± 100 mV, which severely limits the allowable on-chip gain and dynamic range of the amplifier. One of the earliest works in this area proposes to use a reverse-biased diode to clamp the input with the high resistance of the junction depletion region [2]. Ji *et al.* have used internal band-limiting method using diode-capacitor filters to create the low cut-off frequency in [1]. Most of these schemes suffer from optical drift, which reduces their reliability. Recently, Dagtekin *et al.* reported a multi-channel chopper-modulated neural recording amplifier that employs the chopper modulation technique and referencing to an unbiased location in the system to minimize the effects of the DC drift of the neural signals [3]. Only simulated data were presented and the results of the chip performance are not yet published. Finally, Chandran *et al.* report a new DC baseline stabilization technique in which they utilize a sub-threshold NMOS transistor as a high value shunt resistor to polarize the input battery [4]. This resistor in conjunction with the recording electrode capacitance creates the low cut-off frequency of the amplifier. The amplifier is shown to tolerate 400 mV of DC input offset voltage without sacrificing the AC performance. Utilizing this last method, we present a low power two-stage CMOS operational amplifier that provides stable AC gain of 39.5 dB at 1 kHz with a tolerable DC input range of at least 1 V. The amplifier draws nearly 44 μA from a 3 V power supply and is greatly insensitive to ambient light. Section II describes the design of the amplifier. Section III presents and discusses the measurement results and tabulates the performance characteristics of the amplifier for conclusion.

## II. METHODOLOGY

Fig. 1 shows the schematic of the amplifier. A standard two-stage CMOS operational amplifier is utilized in a closed-loop resistive feedback configuration to provide stable AC gain of 39.5 dB set by the resistors' ratio ($R_2/R_1$). At the non-inverting input terminal, a PMOS transistor, $M_p$, is biased in the sub-threshold region to act as a high value resistor in the range of hundreds of mega ohms. This resistor together with the recording probe capacitance, $C_e$, creates a low cut-off frequency below 50 Hz. Resistor $R_g$ is laser programmable so that the PMOS transistor can be always biased in the sub-threshold region even in the presence of ±15% variations in process parameters. No control voltage is applied externally. A two-dimensional common-centroid layout is chosen for the differential input stage to maintain a low input offset voltage. Compensation capacitor $C_c$ is about 4 pF and is present in the circuit layout.

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