Design of low leakage power SRAM using Multithreshold technique

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Abstract*- CMOS scaling technology has leads to sub-threshold leakage, effects of short channel, leakage of gate dielectric and device to device variations increase leakage additionally. In SoC (System on Chip), SRAM cell is occupied in the area of about 90%. It has been implementing by using FinFET, though leakage becomes the considerable main factor in SRAM. In addition, for deep submicron technologies the double gate FinFET devices are became a best option in technology where implemented in deep submicron. By this consideration, we proposed to implement 6T SRAM cell using double gate FinFET (DG FinFET) with independent gate which controlled independently with gates opposite sides that maintains excelling scalability for SRAM. The proposed device is applied using different techniques for leakage reduction namely gated V_{dd} and multithreshold voltage techniques to reduce leakage. Therefore, leakage power in the SRAM cell is decreased and provides better performance. The proposed leakage reduction techniques have been simulated using Cadence in 45 nm technology for FinFET SRAM with independent gate.

***Key words* – CMOS; FinFET; Double gate; DG FinFET; Multithreshold; SRAM**

I. INTRODUCTION

CMOS scaling technology has leads to sub-threshold leakage, effects of short channel, leakage of gate dielectric and device to device variations increase leakage additionally. Nanometer scaling system develops a considerable effect of short channel that produces a number of effects where depletion layer is equal to channel length. Short channel effect (SCE) produced a main effect by its electric fields considerably very high i.e., DIBL. Gate is only controlled this effect. Ultrathin t_{ox} with current drive and very low threshold voltage V_{th} required for maintaining the speed of the device and variations of threshold voltage V_{th} in control while dealing SCE [3]. This effect reduces the slope of the sub threshold which causes variations in V_{th}. Subthreshold leakage and gate leakage currents mainly considered which are generated by SCE where subthreshold leakage generates while $V_{\mathrm{th}} > V_{gs}$ and gate leakage occurs when current passes gate to substrate via oxide layer. To avoid this effects, conventional MOSFET less than 65nm is no more options. Hence, we proposed FinFETs i.e., FET with double gate where opposite of the first gate is connected to second gate so as to reduce the effects of SCE, especially for CMOS low power designs. There are two types of FinFET have been designed such as FinFET with independent gate and tied gate. In FinFET with independent gate, one of the gate acts as switch (on/off) and other gate for adjusting the V_{th} for efficient V_{th} control. It decreases the leakage and therefore decreases the power consumption and enhances the efficiency. To overcome the SCE problem, tied gate FinFET can be used where opposite of the gates are tied with each other. In Microprocessor memory occupied large area in a chip, while leakage current has a significant role thus decreases a small amount of leakage current tends to reduction of large amount in total power. Since SRAM occupied minimum area in a chip with small processing variations and stability by applying low voltages and V_{th} respectively [1, 9]. Therefore, the proposed FinFET approach is desirable for SRAM to extract additional stability and leakage power reduction [2] and also it is most preferable in nano systems with low SCE.

Many techniques has presented for reduction of leakage power. In this research work, we proposed two different techniques in circuit level named as multithreshold leakage and gated V_{dd} [4, 6]. In standby mode NMOS and PMOS functioning as switch to cutoff the supply power thus to reduce the leakage is designed in a leakage reduction technique proposed as multithreshold leakage. It drives high operating speed with small threshold MOSFET, reduction of leakage with high V_{th}. It is observed that by adapting of this technique increases the area for circuit while adding delay and parasitic capacitance at fabrication level. Therefore, we introduced a gated V_{dd} technique where SRAM cell is connected to NMOS transistor. It regulates low threshold and supply voltages by reduction of leakage and minimize the leakage power. When gated V_{dd} is in off additional transistor by combining with SRAM transistors produces a