Current Distribution Control For Parallel Connected Converters: Part II

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In the central-limit control (CLC), the multiloop controls are employed to regulate the output voltage and track the central weighted current, thus equalizing the output current of each converter module (CM). The current distribution error (CDE) between the output current of each CM is used as a criterion in judging system performance. The prediction and simulation results of this control scheme are illustrated. Furthermore, when incorporated with the maximum current limit, the proposed control method can determine the number of required converters in the active state for each load condition. As the result, the efficiency of a system can be increased significantly. A comparison between the performances of a system under master-slave control (MSC) and CLC is given.

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I. INTRODUCTION

In Part I of this article, the master-slave control (MSC) scheme was employed to equalize the current distribution among nonidentical converter modules (CMs) in the parallel connected system. In this control scheme, the master CM is responsible for the voltage regulation and provides the reference current for the slave CMs, while each slave CM is dedicated to tracking the output current of the master. It has been shown that the slave CM can track the output current of the master precisely in steady state. However, because of the lack of the control over the output current of the master CM, there are current overshoots during the transient time. To address this problem here we search for a control scheme which can tightly control the output current of each CM and is capable of reducing the current distribution error (CDE).

In systems of identical parallel connected inverters [1, 2], the difference between I_L/n (which is the total load current I_L divided by the number of operating inverter n) and each individual inverter output current I is detected as the current imbalance ΔI. It was used for the overload output current protection as the main control purpose, not for an optimized uniform current distribution. Additionally, among nonidentical inverters, minimization of the current imbalance ΔI has not been analyzed in previous literature. B. Choi and his colleagues [3] have developed a control strategy for a parallel connected converter system. Some performance characteristics such as system stability, ripple reduction, and transient response in the event of failure of a CM have been analyzed assuming that all the CMs in the system are identical. As mentioned in Part I of this article, Kislovski [6] has analyzed the stability and steady state current deviation of a system under central-limit control (CLC) control, but the overall aspects of a system under the control of CLC incorporated with a maximum current limit technique have not been addressed. In general, little attention has been paid to systems with nonidentical CMs.

Based on the system block diagram, the analysis of the central-limit current distribution control scheme is presented here. We show that this control technique can reduce the CDE among the nonidentical CMs in the system. The control concept can even be extended to systems with CMs of different converter topologies. Instead of tracking the master converter output current as in the MSC control, all the converter output currents in this proposed scheme track the central-limit reference current, which is the total load current divided by the number of active converters connected in parallel. This technique is called the CLC which is described in the following section [4]. Because of the complete control of all CMs output currents, the CLC is able to solve the current overshoot which was present in an MSC controlled system. By using