Effect of Body Biasing Over CMOS Inverter

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Abstract
Threshold level determine the logic '0' or '1' an digital application. Input below threshold consider as '0' and above '1'. At MOS-transistor level threshold can be controlled by adding extra impurity. In this paper a dc bias between body and source terminal used to control the threshold voltage. Threshold voltage increases by forward biasing the body and NMOS and decreases the by reverse bias while threshold voltage of PMOS decreases by forward biasing the body and increases by reverse biasing the body terminal. Zero threshold level can be achieved by body biasing the NMOS which is suitable for high speed switching device. A DC voltage applied between body terminal of CMOS inverter result in shifting up the threshold voltage and result in high power consumption.

Keywords
Threshold Voltage, Body Effect, CMOS Inverter

I. Introduction

In this paper effect of non-zero source-base voltages (VSB) over CMOS inverter has been studied. Conventionally body of PMOS transistor connected with higher potential (Vdd) and body of NMOS transistor connected with Lower potential (Ground). The use of forward biasing the source-substrate junction in metal–oxide– semiconductor transistors to reduce its threshold voltage is a simple method to realize low power complementary metal–oxide–semiconductor integrated circuits. A MOSFET connected in such a way that body to source voltage VBS it is possible to obtain a device with a dynamic threshold voltage Vth. According to the well known body effect VTH increases for a higher reverse VBS while a decrease is expected for an increasing forward VBS [1-3].

The threshold voltage abbreviated as Vth of a MOSFET is usually defined as the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. The formation of the inversion layer allows the flow of electrons through the gate-source junction.

A. Threshold Voltage and Body Effect

The body effect describes the changes in the threshold voltage by the change in VSB the source-bulk voltage. Since the body influences the threshold voltage when it is not tied to the source it can be consider as a second gate and is sometimes referred to as the "back gate"; the body effect is sometimes called the "back-gate effect". Vto is threshold voltage for the zero-substrate threshold voltage differs from Vto only by substrate-bia is a simple function of the material constants and of the source-to-substrate voltage VSB.

$$V_T = V_{T0} + \gamma\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}$$

Where γ is substrate bias effect or body effect [1].Threshold voltage of an enhancement-type n-channel MOSFET is a positive quantity whereas the threshold voltage of a p-channel MOSFET is negative. Threshold voltage of N-channel MOSFETs the threshold voltage is increased by adding extra p-type impurities (acceptor ions) and can be decreased by implanting n-type impurities (dopant ions) into the channel region. Threshold voltage of N-channel MOSFET can be increased by applying positive Vsb alternatively decreased by applying –ve Vsb. Similarly for p-channel MOSFET threshold voltage increased by applying negative Vsb alternatively decreased by applying positive Vsb [3-4].

II. CMOS Inverter

A. Conventional CMOS Inverter

Ideally body of PMOS connected to VDD and body NMOS connected to ground. Voltage transfer characteristics (VTC) indicate that crossing point of output and input curve is threshold voltage of inverter at zero VSB. In the fig shown below [1] crossing point is half of applied input. Ideally half way point indicated threshold between two logic levels [3]

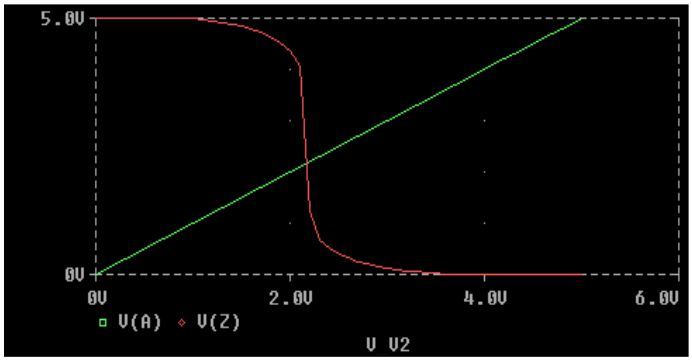

Fig. 1: VTC of Inverter

This threshold between logic levels can be varying according to application. One of the methods is to apply a dc voltage between source and body terminal of MOS transistor. A positive body voltage increased the concentration of minority carrier into substrate of NMOS and helps to form inversion layer. While negative voltage increased concentration of majority carrier and prevents to form inversion layer.

B. PMOS with Body Voltage

A dc voltage applied to the body of PMOS as shown in fig. 2. With negative body voltage majority electron concentration into substrate increased, which prevent the formation of inversion layer. Electron attracted towards inversion layer and neutralized conducting hole. Inversion layer forms at high gate voltage consequently threshold voltage increased. While a positive body voltage increased concentration of minority carrier hole into substrate which helps the formation of inversion layer. Inversion layer can be form at lower gate voltage which results in decrease in threshold voltage. CMOS inverter achieves maximum threshold voltage for negative voltage and threshold decreases with decreasing value of Vsb shown in fig. 3.