Improving Diagnosis Through Failing Behavior Identification

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***Abstract*—Logic diagnosis analyzes the observed failing circuit responses to derive the potential defect sites. This paper describes a method for improving diagnosis through failing behavior identification (FBI). FBI captures defect behavior (i.e., activation conditions of the defect) by identifying the signal lines related to defect activation. This additional information allows the root cause to be estimated in order to improve yield, design quality, and test quality, as well as guide PFA to perform faster defect localization. FBI is accomplished by: 1) deriving the neighborhood states of the defect site, i.e., the actual values on the signal lines within logical or physical proximity to the defect site, and 2) identifying the signal lines that are most relevant to defect activation. The efficacy of FBI is validated using circuit-level and logic-level simulation experiments. The results show that FBI achieves an average accuracy of 94% in identifying signal lines that are relevant to defect activation, a 28% improvement over an existing approach. Moreover, by analyzing the neighborhood states of each defect site reported by logic diagnosis, sites that are not likely to be defective can be eliminated, which leads to improvement in diagnosis resolution. Experiment results show that with little influence on diagnosis accuracy, the number of incorrect defective sites reported by logic diagnosis can be reduced by 64%, on average.**

***Index Terms*—Candidate isolation, defect behavior, failure diagnosis, IC testing, multiple defect, physical failure analysis.**

I. Introduction

EFFICIENTLY identifying the root cause of a nonworking integrated circuit is important for improving yield, test quality, and design quality. Knowledge of the root cause of failure allows corrections in the manufacturing process, adjustments in the test content to maximize the coverage of the actual causes of failure, and modifications in the design to make it less susceptible to certain problems in the manufacturing process. Physical failure analysis (PFA) is typically used to identify the root cause of failure. However, PFA is very time consuming and many times not successful [1]. Therefore, before the application of PFA, logic diagnosis [2] is typically performed to derive a small number of locations that are likely to be the location of the defect. An approach to diagnosis that can accurately identify the defect location is obviously beneficial. It is even more desirable if the defect behavior (i.e., the activation conditions of the defect) can be estimated without PFA. For example, by analyzing various defect behaviors in a failing population together with the behaviors of different types of defects (e.g., bridge, cell, open, and others), the defect-type distribution of that failing population can be estimated [3]. Moreover, test quality can be improved by customizing the test set to match the observed defect behaviors [4].

Due to the tremendous interest in leveraging test data for yield learning, there has been a tremendous amount of interest in diagnosis. Approaches described in [2], [5]–[7] assumed one or more predetermined fault models when deriving defect locations. Such approaches are likely to be misled, however, when the actual defect behavior is different from what is expected by the corresponding fault models. Approaches in [8] and [9] derived potential defect sites without assuming that defects follow a specific fault model, but they do not characterize the defect behavior. The work in [10] instead derived the defect location without assuming a specific fault model, but then used known fault models to deduce the possible defect types. But the limited fault models used only capture a subset of the behaviors exhibited by the known defects [11].

Layout information has been used to improve diagnosis. For example, [12] extracted layout features that are deemed as defect prone and derived the fail rates for each layout feature through volume diagnosis so that yield limiters can be identified. In [13]–[16], design layout was used to extract possible bridge locations that can be used to eliminate impossible bridge candidates reported by logic diagnosis. In the work of [17], the layout of a net was divided into segments to improve the localization of interconnect opens. These methods, however, do not focus on characterizing defect behaviors.

The work of [18] (and subsequent work by others [19]–[24]) described a more generalized approach, referred to as DIAGNOSIX, which locates a defect in a circuit under diagnosis (CUD) without using a specific fault model or defect type and characterizes its behavior by deriving a custom fault model of the defect behavior at the defect location. In that work, the activation conditions for a faulty line f conditionally stuck-at value v is assumed to be a function of the signal lines in the physical or the logical proximity to f, which is

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