Comparison of Direct Growth and Wafer Bonding for the Fabrication of GaInP/GaAs Dual-Junction Solar Cells on Silicon

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***Abstract*—Two different process technologies were investigated for the fabrication of high-efficiency GaInP/GaAs dual-junction solar cells on silicon: direct epitaxial growth and layer transfer combined with semiconductor wafer bonding. The intention of this research is to combine the advantages of high efficiencies in III–V tandem solar cells with the low cost of silicon. Direct epitaxial growth of a GaInP/GaAs dual-junction solar cell on a $GaAs_yP_{1-y}$ buffer on silicon yielded a 1-sun efficiency of 16.4% (AM1.5g). Threading dislocations that result from the 4% lattice grading are still the main limitation to the device performance. In contrast, similar devices fabricated by semiconductor wafer bonding on n-type inactive Si reached efficiencies of 26.0% (AM1.5g) for a 4-cm^2 solar cell device.**

***Index Terms*—Heterojunctions, silicon, wafer bonding, III–V multijunction solar cells.**

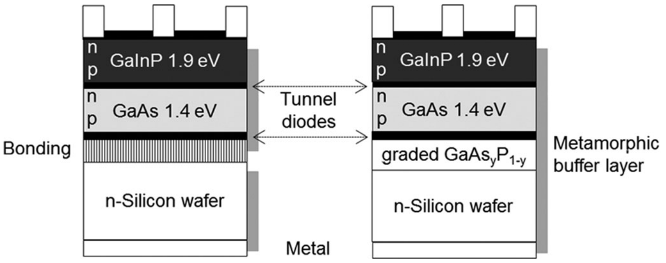

Fig. 1. Schematic of two investigated concepts for the integration of high-efficiency III–V solar cells on silicon. $Ga_{0.5}In_{0.5}P$/GaAs tandem solar cell structure transferred to Si by wafer bonding (left) and direct growth of $Ga_{0.5}In_{0.5}P$/GaAs structure on a GaAsP metamorphic buffer layer on Si (right). Both solar cell structures have an n-on-p polarity and are grown on n-Si. Tunnel diodes are used to connect the top and bottom subcells, as well as the bottom subcell and the n-Si wafer.

I. INTRODUCTION

THE combination of III–V multijunction solar cells and silicon offers many advantages. The high mechanical strength, excellent heat conductivity, nontoxicity, availability in large diameters, and comparably low cost are just some of the most important properties which favor silicon as a semiconductor material. Therefore, the research and development of monolithic III–V solar cells on Si has a long history, but challenges in the fabrication processes, cracking or bowing of films because of high thermal mismatch, and high dislocation densities have so far prohibited the commercial success of this technology [2]. This situation is currently changing for optoelectronic devices like GaN-based LEDs, for which the first commercial products are entering the market. The reasons being that the transition between nonpolar Si and polar III–V crystals is better understood and high-quality nucleation layers of III–V on Si are more widely available today [3]–[7]. Furthermore, the understanding of lattice-mismatched growth has significantly improved over the years [8]–[12]. This also opens new opportunities for III–V multijunction solar cells to be manufactured on Si, especially if high efficiencies can be demonstrated. In this paper, we are investigating two pathways to achieve high-efficiency III–V multijunction solar cells on Si: direct epitaxial growth and thin layer transfer combined with wafer bonding (see Fig. 1). Both of these approaches are viable for industrial applications of III–V on Si solar cells.

Direct epitaxial growth of III–V on Si for solar cells was successfully developed in the 1990s, for example, by Umeno *et al.* [13] and Yang *et al.* [14]. They proved efficiencies up to 20% for AlGaAs/Si devices under AM0. Ringel *et al.* were following a different approach by combining SiGe templates grown by chemical vapor deposition with MBE growth of a GaAs or GaInP/GaAs solar cell structure [15]–[18]. The best devices showed a total area efficiency of 16.8% under AM1.5g conditions. More recently, GaP nucleation layers on Si with high crystalline quality and low density of antiphase domains (APDs) became available [3], [4], [7], and publications are concentrating

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