LEVEL SHIFTER DESIGN FOR LOW POWER APPLICATIONS

Manoj Kumar[1], Sandeep K. Arya[1], Sujata Pandey[2]

[1]Department of Electronics & Communication Engineering
Guru Jambheshwar University of Science & Technology, Hisar, India,
manojtaleja@rediffmail.com, arya1sandeep@rediffmail.com
[2]Amity University, Noida, India
spandey@amity.edu

ABSTRACT

With scaling of Vt sub-threshold leakage power is increasing and expected to become significant part of total power consumption.In present work three new configurations of level shifters for low power application in 0.35µm technology have been presented. The proposed circuits utilize the merits of stacking technique with smaller leakage current and reduction in leakage power. Conventional level shifter has been improved by addition of three NMOS transistors, which shows total power consumption of 402.2264pW as compared to 0.49833nW with existing circuit. Single supply level shifter has been modified with addition of two NMOS transistors that gives total power consumption of 108.641pW as compared to 31.06nW. Another circuit, contention mitigated level shifter (CMLS) with three additional transistors shows total power consumption of 396.75pW as compared to 0.4937354nW. Three proposed circuit's shows better performance in terms of power consumption with a little conciliation in delay. Output level of 3.3V has been obtained with input pulse of 1.6V for all proposed circuits.

KEYWORDS

CMOS, delay, level shifter, power consumption and stacking technique.

1. INTRODUCTION

With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become major design consideration for VLSI circuits and system [1], [2]. With increase in power consumption, reliability problem also rises and cost of packaging goes high [3]. Power consumption in VLSI circuit consists of dynamic and static power consumption. Dynamic power has two components i.e. switching power due to the charging and discharging of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [4]. The static power of CMOS circuits is determined by the leakage current through each transistor. Power consumption of VLSI circuits can be reduced by scaling supply voltage and capacitance [4]. With the reduction in supply voltage, problems of small voltage swing, insufficient noise margin and leakage currents originate [5]. With the development of technology towards submicron region leakage power has become significant component of total power dissipation [6], [7]. Static power component of power consumption must be given due consideration if current trends of scaling of size and supply voltage need to be sustained.

In System on chip (SoC) design, different parts like digital, analog, passive component are fabricated on a single chip and needs different voltages to achieve optimum performance. Level converters are used to convert the logic signal from one voltage level to other level and are the significant circuit component in VLSI systems. Level shifters are also important circuit component in multi voltage systems and have been used in between core circuits and I/O circuit. Various design for level shifters have been reported in literature with single and dual supply [8]-