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0.5 V fully differential current conveyor using bulk-driven quasi-floating-gate technique

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Abstract: This study presents a new low-voltage (LV) supply and low-power consumption bulk-driven quasi-floating-gate fully differential current conveyor (BD–QFG-FDCCII) active element which is suitable for LV signal processing applications. The bulk-driven technique is used to achieve LV supply as low as a 0.5 V and extended input voltage swing. On the other hand, the quasi-floating-gate technique is used to achieve high-frequency performance. To prove the workability of the proposed circuit, new voltage-mode biquadratic filter and fifth-order leap-frog low-pass filter using BD–QFG-FDCCIIs as active devices have been designed and illustrated in this study. The functionality of the proposed circuits is demonstrated through PSPICE simulations using Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 µm n-well complementary metal–oxide–semiconductor technology with a 0.5 V supply voltage and a power consumption of 16.1 µW.

1 Introduction

In the year 2000 a new current-mode active building block, the so-called fully differential current conveyor (FDCCII), has been introduced [1]. The FDCCII is designed to improve the dynamic range and to suppress all undesirable common-mode signals. This active element has four y-terminals, plus/minus x-terminals and plus/minus z-terminals; hence with a single device the arithmetic operation capability of voltage signals and addition/subtraction of current signals can be easily obtained. Therefore, a number of analogue signal processing applications using FDCCII as active element have been presented in many technical literatures [2–11]. However, the majority of these publications have used the FDCCII that proposed in [1]. Although, this popular FDCCII provides high performance for analogue signal processing, the supply voltage of ±1.65 V is used with high power consumption.

For the time being, there is a great demand on designing and implementing of low-voltage (LV) and low-power (LP) integrated circuits such as active elements presented in [12–43]. This demand is based on the fact that LV LP circuits are needed in portable equipment, smart phones, tablet computers and neural network, especially in biomedical and bioelectronics systems. Unfortunately, there is no ultra-LV and LP FDCCII available in the open literature. Although, there are two FDCCIIs using LV LP techniques such as floating-gate and bulk-driven (BD) techniques presented in [28, 31], the supply voltage of these circuits is still ≥1 V.

Therefore, the aim of this paper is to design a new LV LP BD quasi-floating-gate fully differential current conveyor (BD–QFG-FDCCII) for LV LP integrated circuit applications such as the ones used in bioelectronics, biosensor and biomedical systems. The BD quasi-floating-gate (BD–QFG) is conceptually a combination of the BD metal–oxide–semiconductor (MOS) transistor technique and the quasi-floating-gate (QFG) MOS transistor technique into a single MOS transistor [36–41]. This technique shows the positive aspects of the BD technique such as LV and rail-to-rail input voltage swing, and the positive aspects of QFG technique such as high value of transconductance; hence it compensates for weakness of BD technique, resulting in high-frequency performance of the proposed LV LP devices.

The proposed BD–QFG-FDCCII is designed using 0.18 µm complementary MOS (CMOS) technology and a supply voltage of 0.5 V. The proposed BD–QFG-FDCCII is used to realise voltage-mode biquadratic filter and fifth-order leap-frog low-pass filter as example applications. The PSPICE simulation is performed to examine the performance of the new CMOS structure of this active building block.

2 BD–QFG MOS transistor technique

In the area of analogue circuits design, the signal-to-noise ratio (SNR) and dynamic range (DR) are major requirements that should be maintained as large as possible. However, in practice, reducing the supply voltage commonly leads to reduce the SNR and DR values, which causes a big obstacle facing LP LV circuit designers. The second obstacle for designing LV LP analogue circuits is the threshold voltage of the MOS device which is not decreased at the rate as the supply voltage, and is not expected to be decreased more than what is available today; although the feature size of CMOS technology is continuously decreased to scale down.

Subsequently, there are among variety of special techniques that used to achieve acceptable circuit performances under LV LP condition such as floating-gate (FG), BD, subthreshold region (weak inversion) and QFG MOS transistor; for example [12–34]. Unfortunately, these special techniques suffer from limitation of transconductance value. The limitation of transconductance value commonly means the limitation of operating frequency of the devices. It is well-known that the transconductance value of the conventional gate driven (GD) MOS transistor operating in saturation region is the best choice for circuit design techniques, but it has generally been acknowledged that such a driven technique is incapable of circuit operating under ultra-LV condition.

If the transconductance values have been expressed as follows: GD (g_m), QFG ($g_{m\text{-QFG}}$), FG ($g_{m\text{-FG}}$) and BD (g_{mb}) MOS transistors, then the relationship between them can be expressed as $g_m > g_{m\text{-QFG}} > g_{m\text{-FG}} > g_{mb}$ [35, 36]. This means that the value of the operating frequency of BD technique is the lowest because it