Design, Package, and Hardware Verification of a High Voltage Current Switch

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***Abstract*—In this paper, an attempt has been made to demonstrate various package design considerations to accommodate series connection of high voltage Si-IGBT (6500V/25A die) and SiC-Diode (6500V/25A die). The effects of connecting the cathode of the series diode to the collector of the IGBT versus connecting the emitter of the IGBT to the anode of the series diode have been analyzed in regards to parasitic line inductance of the structure. Various simulation results have then been used to redesign and justify the optimized package structure for the final current switch design. The package is fabricated using the optimized parameters. A double pulse test-circuit has been assembled. Initial hardware results have been shown to verify functioning. The main motivation of this work is to enumerate detailed design considerations for packing a high voltage current switch package.**

Keywords— Wide-Bandgap, Current Switch, High Voltage, Series IGBT and Diode, Silicon Carbide, Packaging.

I. INTRODUCTION

The current switch (series connected switch and diode) has found its application in various current source based converters [1]-[5]. The main advantages of using current-source based topologies can be linked to the fact that these converters usually use less number of active switches, have a more rugged natural protection (owing to the series diode), are well suited for zero-current and zero-voltage based soft switching, etc [6]-[7]. These converters are usually made using thyristors with external commutation circuits, albeit at low switching frequency. The frequency of operation can be pushed to significantly higher values by using faster devices, like IGBTs. With the advent of Silicon-Carbide Devices, singular power electronic devices can now operate beyond 10kV-15kV levels [8]-[12]. This effectively reduces the number of series connected components in the circuit, but drastically increases the dielectric and thermal stresses that develop within the power module. The non-sinusoidal nature of this stress which is punctuated with high dV/dt and dI/dt, leads to several steep constraints in terms of parasitic series inductance, shunt stray capacitance, capacitive coupling, thermal conduction, etc [13].

As previously mentioned, the current switch has an additional diode in series with the regular active switch. Packaging this structure comes with an inherent problem of dealing with peak positive (owing to the switch) and negative (owing to the diode) voltage stress within a span of less than 100µs. This is considerably larger than regular switches for the same terminal voltage rating. In order to understand fully how these non-conventional stresses affect the current switch packaging, and therefore the overall switch operation, multi-physics simulations have been performed for various layouts of this series diode and regular switch topology based on a material selection that is capable of the required dielectric strength. Physics based accurate device models have been studied with estimated parasitic parameters in SIMPLIS-SIMETRIX. Various cross simulation results have then been used in an iterative fashion to redesign and analyze the optimized package structure for the final current switch design. The paper is divided into several subparts. First, the basic structure and common testing practices of current switch are enumerated. Two different approaches of fabrication are discussed. MAXWELL and Q3D based simulations depicting the voltage/current distribution in the module and extraction of various parasitic parameters are then studied. 3D Printed Package housing and initial double pulse results have been shown. Finally, the paper is concluded depicting the major critical design parameters and proposed design considerations.

II. PRINCIPLE STRESS AND OPERATIONS OF CURRENT SWITCH

As in most power electronic circuits, the switches usually undergo hard-switching states. In hard switching transitions, the device undergoes a state when both its voltage and current are non-negligible. This state can last for as low as sub 100ns to as high as above 100us. This leads to increased amount of power loss in the device and the overall converter. It is therefore essential to study the ill effects of this stress in the package. The main motivation of this part of the work is to demonstrate the typical stress in terms of turn-on and turn-off voltage and current as seen in the device during such hard switching conditions. Fig. 1 shows the test circuit schematic. In this test, Vin is set to 1000V. At first S1 is turned on and consequently, the inductor (Lo) current rises linearly. At some point of time S2 is turned on. As the series connected diode (D2) is reverse biased, S1 continues to conduct. At a following point in time, S1 is turned off and the non-zero inductor current is forced to flow through S2 and D2. A similar gating-pulse is again passed through S1 and S2. This forms a complete double pulse test. Overall, this results in hard turn-on and turn-off of the switch S1. Fig. 2 and 3 show the test circuit with parasitic inductance and capacitance