A Modified Folded Multi-LSB Decided Resistor String Digital to Analog Converter

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Abstract— **This work proposes an improved folded multi-LSB decided resistor string digital to analog converter which has lower number of resistors. The nonlinearity calculations are done for this design in order to better analyze the resistor mismatch. Since no buffers are employed to this architecture, the proposed circuit has ameliorated performance in compare with the conventional digital to analog converters. As the buffer is omitted from this topology, the offset problem and the bandwidth limitations are solved.**

Keywords- digital to analog converter; folded multi-LSB decided; resistor string.

I. INTRODUCTION

The converters are the main building blocks of the electronic fields especially video processing. Different digital to analog converter (DAC) structures have been designed with various pros and cons. Binary weighted DAC, R-2R ladder DAC, current steering DAC and resistor string DAC are the most common DACs that are used in many applications [1]. Resistor string DAC is one of the first MOS DACs that works based on activating the numbers of switches, which are controlled by digital inputs, and selecting some segmented resistor strings among the total resistors, that shows the analog quantity proportional to the digital input code. Since it needs large number of switches, resistor string DAC with decoder has been presented. By using decoder in the resistor string DAC architecture the number of switches are reduced to 2^N. Despite the best of intentions that it has, the topology of the decoder becomes complicated as the resolution is increased. Therefore the folded resistor string converter was designed that its performance is very similar to that of digital memory [1]. For example in a 4-bit DAC instead of using one 4 to 16 decoder, two 2 to 4 decoders are used. As shown in Fig. 1 each decoder activates one of its four lines. The activation lines of one of the decoders are called word lines while those of other decoder are named bit lines. Each word and bit line activates one transistor and selects one tap of segmented resistors, which is transferred to the analog output [2].

Although the folded resistor string converters reduce the total number of transistors to $2\sqrt{2^N}$, the accuracy of the converter is decreased by enhancing the speed [1]. When one of the word lines becomes activated, the bit lines change their level to a new one and in this situation two or more bit lines are fed to the output buffer.

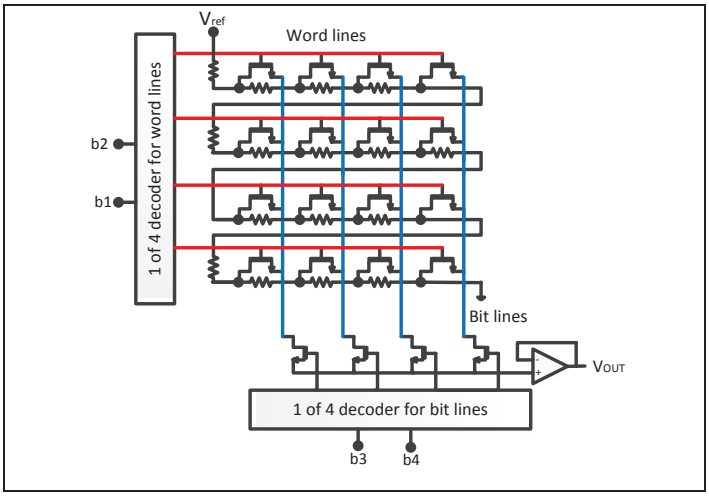

Figure 1. The proposed folded multi-LSB decided resistor string DAC.

To improve the performance of the resistor string DAC an additional interpolating resistor string is employed [3]. The multiple resistor string DAC, if increases the accuracy, has a mismatch problem between two stages. Several methods have been proposed to eliminate the buffer and compensate the effect of interpolator loading on the coarse stage. Buffer resistors which replace the buffer amplifiers, although improve the speed and chip area, require additional control switches [4].

By employing current source isolation technique, the extra logic for controlling the switches of buffer resistors is eliminated, but still there is the mismatch limitation in sinking and sourcing currents [5]. Offset switching technique can also ameliorate the resistance of the switch and capacitive loading effect on the coarse stage, but it can't preferably isolate coarse resistor string from the interpolating resistor stage [3]. Level shifters in the multiple resistor string DAC not only capacitively isolate two resistor stages, but also significantly reduce the ohmic resistance of the switches [3]. Drain- source voltage matching of the NMOS and PMOS transistors in the level shifters is the drawback of this topology.

Folded multi-LSB decided resistor string DAC uses main and sub-resistors in one stage to ameliorate the isolating

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