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DESIGN HIGH SPEED, LOW NOISE, LOW POWER TWO STAGE CMOS OPERATIONAL AMPLIFIER

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ABSTRACT

The objective of this paper is to design a Low-Voltage, Low-Power and High-Gain Operational Amplifier used for high speed compensated CMOS op-amp which specifies open loop circuit parameters to obtain enhanced gain, settling time and closed loop stability An Op-Amp is designed in a 0.18 µm standard digital CMOS Technology The low noise high speed Op-Amp is designed using 180nm CMOS technology and exhibits. Slew rate to 17 V/ms and gain-bandwidth product to 63 MHz, gain margin 80db, phase margin 77 db Performance of an op-amp at supply voltage 1.8V .

Keywords: Two Stage OP-Amp high speed low noise OP-Amp Circuit , Op-Amp, Phase Margin, gain margin, precision circuit.

INTRODUCTION

The designing of high performance analog integrated circuits is becoming most essential with the continuous trend towards the reduced supply voltages and transistor channel length. MOS is most success among all because it can be scaled down to smaller dimensions for higher performance. The size can be reduced to micrometer or nanometer for getting higher performance. On scaling down the Transistor size the most important advantage iswe can integrate more number of transistors on the same size and we can get a faster amplifier compared to previous one. This leads to continuous growth of the processing capacity per chip and operating frequency. To achieve high gain with continued scaling in CMOS fabrication processes, use of multiple stage op-amps has become indispensable. Many applications require high-speed analog-to-digital converters (ADCs) due to increasing data rates. Hence, they require high accuracy op-amps with very high dc gain and high unity gain frequency in order to meet both accuracy and settling requirements of the system. The op-amp is one of the most important building blocks of the analog circuit technology.

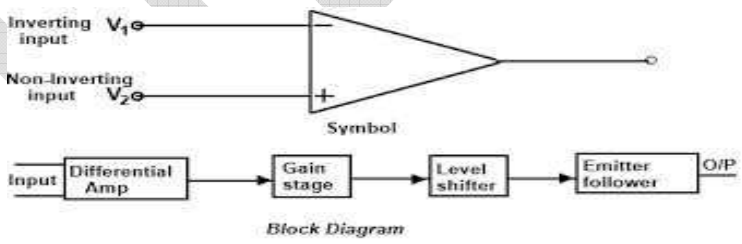

Fig 1: Block diagram of op-amp

Almost all amplification and filtering functions can be realized using op-amps. Several fundamental issues and trade-offs exist when selecting an optimal Amplifiers are the most common building blocks. So as the transistor channel length and power supply is reduced then the design of Op amps face continuous challenge. Due to different aspect ratio (W/L), there is a trade off among speed, gain, power and the other parameters. The implementation of a CMOS OPAMPs that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this paper is to propose accurate equations for the design of high- gain2 staged CMOS op-amp.