RAM and TCAM Designs by Using STT-MRAM

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***Abstract*—Spin-transfer torque magnetic random access memory (STT-MRAM) is a prospective candidate for cache and main memory designs. However, the reliable revision of magnetization using current requires high current density, which is hardly affordable in aggressive scaling-down technology node. Nano-ring shaped magnetic tunneling junction (NR-MTJ) remarkably reduces STT programming current density, as indicated by theoretical analysis. In this paper, we first introduce the fundamental of STT technology and describe the NR-MTJ's structure and characteristics. The design and implementation of a 4Kb STT-MRAM with NR-MTJs, and a TCAM design for high speed and robustness are then demonstrated.**

***Index Terms*—Spin-transfer torque, magnetic tunnel junction, random access memory, ternary content addressable memory.**

I. Introduction

The demand for memory capacity and bandwidth in modern computing systems grows dramatically to accommodate the requirement of emerging applications such as big data, Internet-of-Thing (IoT), machine learning, etc [1]. Thus, many nonvolatile memory (NVM) technologies are investigated.

Spin-transfer torque (STT) memory is a type of magnetic memory technology that directly uses electrical current to program its storage elements – magnetic tunneling junctions (MTJs) [2], [3]. It possesses attractive characteristics, including nonvolatility, nanosecond access time, small footprint, and compatibility to CMOS process. The use of MTJs in many memory structures have been developed in both academia and industrial researchers, such as random access memory (RAM), ternary content addressable memory (TCAM) and nonvolatile latches. Moreover, advanced structures, e.g., multi-level cell (MLC) that holds 2-bit data [4], [5] and spin-orbit torque (SOT) MTJ with 3 terminals [6] were proposed to further performance improvement. Nevertheless, there are some technical challenges in commercializing STT-RAM technology. Particularly, the tradeoff between high programming current density and fast access speed, and the reliability due to operational disturbance and process variations still need a lot of engineering efforts [7], [8].

Our research focuses on improving the performance and robustness of STT technology and enabling its use in memory and logic applications. Two examples will be presented in this paper: the design and implementation of a 4Kb STT-MRAM with innovative 100nm nano-ring shaped magnetic tunneling junction (NR-MTJ), and a TCAM design based on STT-MRAM for high speed and robustness. The purpose of this work is to provide our readers an introductory overview of STT technology from device, circuit, design methodology, and application perspectives.

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II. STT-RAM Preliminaries

A. STT Switching Mechanism

Fig. 1 illustrates the vertical stacking structure of a MTJ. An oxide layer is sandwiched between two ferromagnetic layers, namely, the *free* layer and the *reference* layer. A pinning thin film fixes magnetization of the reference layer, while the magnetization vector in the free layer can be toggled as its name implies. Different relative angles between magnetization vectors in these two layers result in distinguished tunneling magnetoresistance. Tunneling magnetoresistance ratio (TMR) is used to represent the relative distance between the highest and lowest resistances of a single MTJ device, such as

$$\mathrm{TMR} = \frac{R_H - R_L}{R_L} \times 100\%. \quad (1)$$

Accordingly, binary data '1' and '0' are stored as the highest and the lowest resistances, respectively.

An STT-MTJ uses current to manipulate its magnetization direction and change the resistance state [2], [3]. Limited by the spin-torque efficiency, a high current density J_c ($\sim 10^6 A \cdot cm^{-2}$) is required [9], [10]. Conventional MTJ are made of an elliptical shape (called as "E-MTJ" in this paper), where unsymmetrical long and short axises form shape anisotropy to maintain thermal stability. In a write operation, the writing current I_{write} shall be greater than $I_c = A_{ellipise} \times J_c$. Where, $A_{ellipise} = \pi ab$. $A_{ellipise}$ is the ellipse area. a and b denote the lengths of long and short axises, respectively.

B. Nano-Ring MTJ

Fig. 2 illustrates NR-MTJ and its current-induced switching between two resistance states. An NR-MTJ is composed of the same vertical stack structure as the E-MTJ [11]. However, NR-MTJ has a hole in its center, forming a vortex magnetization

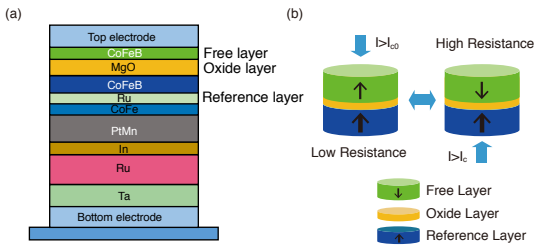

Fig. 1. The MTJ structure: (a) vertical stacking structure; (b) the free layer, oxide layer and reference layer (arrows represent magnetization vectors).